Millimeter-Wave CW IMPATT Diodes and Oscillators

THOMAS A. MIDFORD, MEMBER, IEEE, AND ROBERT L. BERNICK, MEMBER, IEEE

Invited Paper

***Abstract*—This paper summarizes the current state of the art of silicon CW millimeter-wave IMPATT diodes and oscillators in the frequency range from 30 to 250 GHz. Design procedures, fabrication, and packaging technology are reviewed, and the current performance of diode oscillators is reported. A brief account of present device reliability is also presented. The contrast between maturing device technology below 100 GHz and largely laboratory-based technology at higher frequencies is discussed. Finally, a prognosis of future developments is offered.**

I. Introduction

OVER THE PAST several years, significant progress in output power and efficiency has been achieved with IMPATT diodes and oscillators operating at frequencies from 30 to 300 GHz. These results have been obtained in both the CW and pulsed modes of operation. From silicon double-drift/flat-profile devices, pulse powers of 23 W at 35 GHz, greater than 15 W at 94 GHz, and 520 mW at 217 GHz have been obtained [1]. Similar silicon devices operating in the CW mode have produced 2.25 W at 40 GHz, 980 mW near 100 GHz, and 50 mW at 220 GHz. All of the latter devices employ type-IIA diamond heat sinks. These results clearly place silicon IMPATT diodes as the premier solid-state device for generation of millimeter-wave power. This paper describes device design and fabrication technology as well as packaging and circuit developments which have led to these results. In addition, a prognosis of future developments is presented.

In overview, silicon millimeter-wave IMPATT diode technology may be divided into two general regions based on frequency. This division is shown schematically in Fig. 1. Devices operating at frequencies below roughly 100 GHz have a technology which is beginning to mature. Devices throughout this frequency range (practically from *X* band through 100 GHz) are fabricated using a common materials, process, and packaging technology. On the other hand, devices operating at frequencies above 100 GHz are still largely in the laboratory or research stage with a technology more difficult and different in many respects from that of the lower frequency devices. Also shown in Fig. 1 is atmospheric attenuation as a function of frequency in the millimeter-wave region. Note that, in many instances, millimeter-wave user frequencies are determined by the low attenuation atmospheric windows, for example, those at 35, 94, and 140 GHz. Currently, much

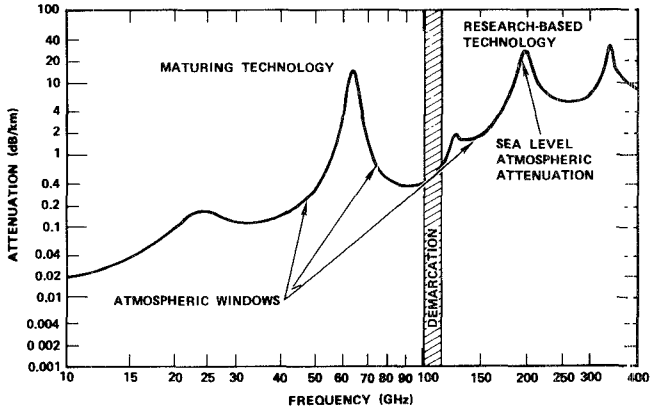


Fig. 1. IMPATT diode technology referenced to atmospheric attenuation windows.

TABLE I
COMPARISON OF SILICON IMPATT TECHNOLOGY BELOW AND ABOVE 100 GHz

	Devices Below 100 GHz	Devices above 100 GHz
1. Profile Formation	Multiple epitaxy Diffusion	Epitaxy Ion Implantation Diffusion
2. Wafer Thinning	Etch to 15-30 microns	Special techniques required to thin to 5-10 microns or less
3. Contact metallurgy	Multicomponent e.g., chromium-platinum-gold	Chromium-platinum-gold
4. Heatsinking	Copper, silver or type II-A diamond	Copper, silver or type II-A diamond
5. Chip diameter	Up to 100 microns or greater	Ranges approximately from 10 to 30 microns
6. Package configuration	Hermetically sealed, ceramic or quartz ring insulator	Open standoff or wafer package
7. Process and package yield	Moderate	Low
8. Screening procedures	Developed for certain devices at particular frequencies	Not yet developed
9. Reliability	Some life testing and failure analysis to support MTBF predictions. Single failure mode most common.	No work

Manuscript received August 1, 1978; revised December 10, 1978. This work was supported by the U.S. Air Force Avionics Laboratory, Wright Patterson Air Force Base, OH.

T. A. Midford is with the Hughes Aircraft Company, Torrance Research Center, Torrance, CA 90509.

R. L. Bernick is with the Hughes Aircraft Company, Culver City, CA 90230.

0018-9480/79/0500-0483$00.75 ©1979 IEEE

component and, to a lesser degree, system development activity is in progress at these frequencies. Note then that IMPATT diodes at 35 and 94 GHz fall in the maturing technology region, while devices at 140 GHz and higher frequencies do not. Table I shows a comparison of the principal elements of silicon IMPATT technology for devices above and below 100 GHz. Most of the items included in Table I are self-explanatory, and many are expanded later in this paper.

II. IMPATT Diode Design

A. Doping Profile

A double-drift-region (DDR) flat doping profile is most commonly used for millimeter-wave silicon IMPATT diodes. The DDR profile consists of a p^+-p-n-n^+ multilayer structure as shown in Fig. 2. Also shown in Fig. 2 is the electric field profile at avalanche breakdown. The p- and n-type layers contain the device active region. This structure was proposed by Scharfetter *et al.* [2]. It is superior to the original p^+-n-n^+ single-drift-region (SDR) IMPATT structure because of the increased power generating capability due to two drift zones and because the junction area of a DDR diode can be larger than an SDR diode for a given impedance level. Calculations have indicated that the expected output power for a DDR diode is greater by a factor of approximately 2.7 than for a corresponding SDR device [3]. Ideally, because of differences in the silicon electron and hole ionization rates and saturated drift velocities, the profile should be asymmetric with the p-type layer somewhat narrower.

When the diode is operated under reverse bias, the active region widens due both to space-charge and temperature effects. The doping levels and thicknesses of the p- and n-type regions should be chosen such that the electric field just punches through to the p^+ and n^+ contact regions under operating conditions. If either the p- or n-type region is too wide for the doping level, some of the high resistivity material will remain undepleted and will contribute to a parasitic series resistance with reduced RF power and efficiency. Conversely, if the active region is too narrow so that the electric field punchthrough is excessive, efficiency is also reduced because of widening of the avalanche region [4].

The thickness of the active region and corresponding doping levels are chosen based on transit-time considerations. Both theoretical small- and large-signal calculations and experimental results aid in selecting the appropriate values. Scaling laws are sometimes useful in translating the design of an IMPATT from one frequency to another [5]. A first-order diode design can be obtained based on the small-signal analysis of Misawa [6]. The device small-signal negative Q can be used as a rough figure of merit in that it gives information on oscillation threshold and rate of buildup. In this sense, a smaller magnitude of Q is preferable [6], [7]. Fig. 3 shows the calculated device small-signal conductance, susceptance, and Q plotted as a function of frequency for a diode designed for operation near 40 GHz. The diode doping level is $6\times10^{16}/\text{cm}^3$ in

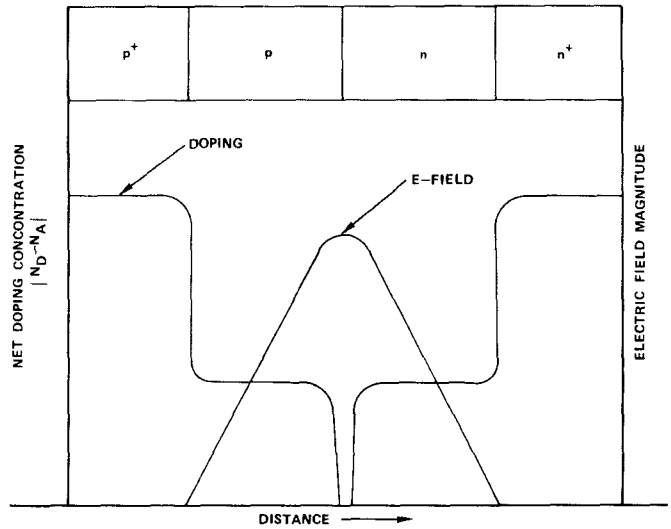


Fig. 2. Double-drift IMPATT diode profile.

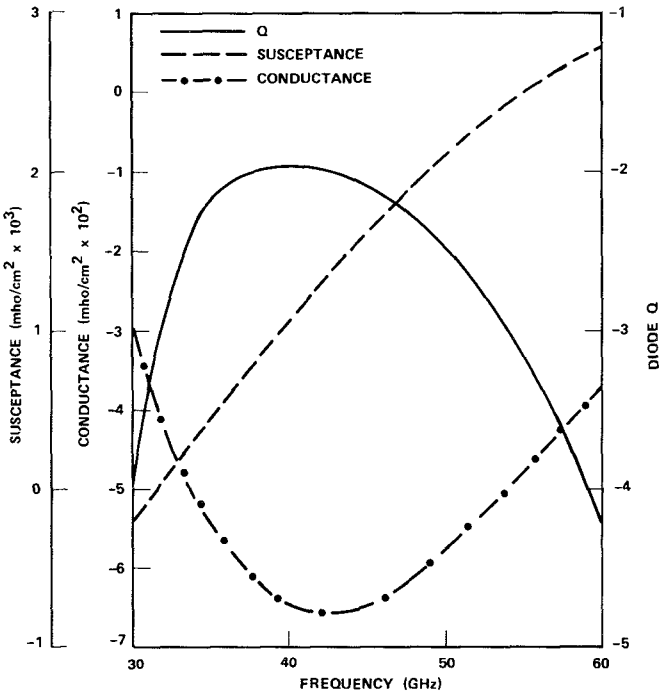


Fig. 3. Calculated small-signal conductance, susceptance, and Q as a function of frequency for a 40-GHz DDR IMPATT diode.

both the n- and p-type regions. The current density is 1.0×10^4 A/cm^2, and the junction temperature is 250°C, which are near typical operating values. The drift velocities reported by Canali *et al.* [8], [9] and the ionization rates of Grant [10] were assumed. Note that the magnitude of small-signal conductance has a maximum, and the magnitude of Q has a minimum near 40 GHz.

To examine the effect of doping asymmetry, additional profiles have been studied at the small-signal level. Seven profiles, each with a value of N_{eff} approximately equal to $3\times10^{16}/\text{cm}^3$ were analyzed. (N_{eff} is the apparent doping level obtained when capacitance–voltage measurements are performed on a double-drift structure. Its value for a flat profile is given by $N_{\text{eff}}^{-1}=N_A^{-1}+N_D^{-1}$ where N_A and N_D are, respectively, the net acceptor concentration in the

TABLE II
SUMMARY OF SMALL-SIGNAL CALCULATIONS

Case	N_D ($\times 10^{16}/cm^3$)	N_A ($\times 10^{16}/cm^3$)	N_{eff} ($\times 10^{16}/cm^3$)	Minimum $\|Q\|$	Freq. at Minimum $\|Q\|$ (GHz)
I	6.0	6.0	3.0	1.95	40
II	6.5	5.5	3.0	2.00	40
III	5.5	6.5	3.0	1.94	40
IV	8.0	5.0	3.1	2.18	39
V	5.0	8.0	3.1	2.01	40
VI	12.0	4.0	3.0	2.99	37
VII	4.0	12.0	3.0	2.30	38

TABLE III
DESIGN PARAMETERS FOR MILLIMETER-WAVE CW DDR IMPATT'S

Approximate Frequency (GHz)	$N_D = N_A$ (cm^{-3})	Active Region Width (μm)	Diode Breakdown Voltage (V)
40	6×10^{16}	1.2	28
60	1.0×10^{17}	0.90	22
94	1.8×10^{17}	0.60	16
170	4.5×10^{17}	0.32	10
225	5.5×10^{17}	0.25	8.5

p region and the net donor concentration in the n region.) In each case, the current density was taken as 10^4 A/cm^2, and the temperature is 250°C. Results for the seven cases are summarized in Table II.

Of the profiles studied, case III has the lowest magnitude of Q around 40 GHz. However, the symmetrical structure (case I) and the other structures with the least asymmetry (cases II, IV, and V) show only a small increase in this parameter. Note that the asymmetric profiles with $N_A > N_D$ result in a lower $|Q|$ than the corresponding cases with $N_D > N_A$.

The conclusion is that for a given N_{eff}, small deviations in the values of N_D and N_A from the symmetric case do not have a substantial effect on the small-signal operating parameters. It must be noted, however, that these small-signal results do not take account of the effect of undepleted epitaxial material during device operation.

Design values for doping level and active region widths appropriate to symmetric DDR CW IMPATT's for frequencies ranging from 40 to 225 GHz are shown in Table III. These values are based both on theoretical analyses and on experimental results.

B. Thermal Design

Double-drift-region IMPATT diodes intended for CW operation are thermally limited. Thus it is essential to have the junction-to-ambient thermal resistance minimized in order to achieve high-power results. Both metallic (copper or silver) and type-IIA diamond are conventionally used heat-sink materials. However, a significant thermal advantage is gained by using type-IIA diamond heat sinking. The thermal resistance can be calculated using a simple thermal model consisting of a silicon diode chip mounted on a layered heat sink as shown in Fig. 4. The layer of gold is a bonding layer. The total thermal resistance θ is given as

$$\theta = \theta_C + \theta_{HS}$$

where θ_C is the contribution due to the silicon and the thin layers of contact metallization between the junction and heat sink and θ_{HS} is the contribution from the two-layer heat sink. The value of θ_{HS} has been obtained for the case where the thermal conductivity in each layer is independent of temperature [11]. The thermal conductivity of diamond is known to be a function of temperature. However, a constant value of 9 W/cm·°C has given reasonable agreement between calculated and experimental values of θ.

Using the method described above, the thermal resistance for DDR diodes designed for operation near 94 GHz and mounted on both copper and type-IIA diamond heat sinks has been calculated as a function of pill diameter. Results are plotted in Fig. 5. Also shown are experimental values for θ measured for DDR diodes on copper and diamond heat sinks. For a diode diameter of 40 μm, the value of θ for diamond is roughly 55 percent of the corresponding value for copper. Thus for a fixed output

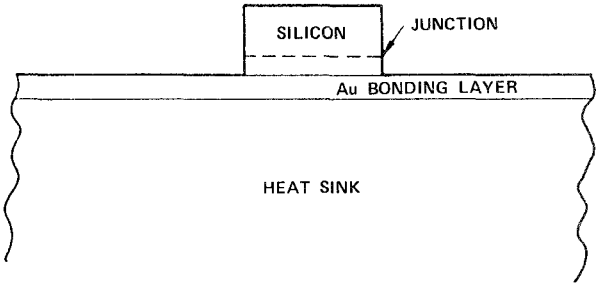


Fig. 4. Thermal model.

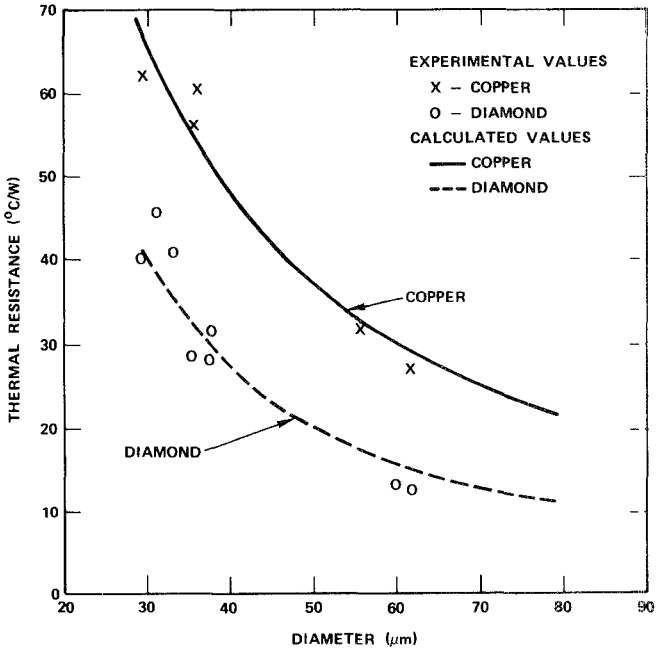


Fig. 5. Thermal resistance as a function of diode diameter.

power and efficiency, the temperature rise over ambient for diamond heat sinking is only about 55 percent of the corresponding rise for copper. Conversely, for a fixed junction temperature and efficiency, the output power can be increased about 80 percent by using diamond rather than copper. However, efficiency is also enhanced with diamond heat sinking [12] so that the actual power increase can be even greater.

III. Device Technology

A. IMPATT Profile Formation

The devices described in this work employ p^+-p-n-n^+ doping profiles which are formed in one of two ways. The first method, employed primarily for diodes operating at frequencies below 100 GHz, is to grow epitaxially n- and p-type regions in sequence on a low-resistivity (~0.002 Ω·cm) arsenic doped substrate. The p^+ contact layer is formed by a shallow low-temperature boron diffusion. In the second technique, which is used for fabricating higher frequency devices, an n-type region is first epitaxially grown on the arsenic doped substrate wafer. Next, the p layer is formed by overcompensating a portion of the n layer with multiple energy ion implants of boron. The p^+ contact layer is then formed using boron diffusion. Fig. 6 illustrates such a profile for a 225-GHz DDR diode. Currently, the first procedure is used in IMPATT diodes operating at frequencies below 100 GHz, while the second, employing ion implantation, is used for fabricating higher frequency devices. In general, ion implantation provides a higher degree of precision in fabricating very thin multiple-layer structures than multiple epitaxy. The latter, however, is easier to implement and is completely satisfactory for lower frequency devices.

Double-drift profiles formed by ion implantation are subject to some degradation as a result of ion straggling effects in the vicinity of the p-n junction. This effect has been studied analytically. Two doping profiles are shown in Fig. 7. The first structure (profile 1) is an idealized symmetric double-drift-region (DDR) profile designed for operation near 225 GHz. The profile consists of uniformly doped p and n regions, each doped at a level of 5.1×10^{17} cm^{-3}. The second structure (profile 2) is a more realistic representation which contains deviations from the ideal profile which are characteristic of ion-implantation straggling effects. The grading of profile 2 at the p-n junction causes the electric field to be rounded at the peak and results in a wider active region with a lower peak field. This effect in turn leads to a relative widening of the avalanche region. The small-signal admittance characteristics for the two profiles have been calculated as a function of frequency and are plotted in Fig. 8. For these results, the current density was 1.19×10^5 A/cm^2 and the temperature 225°C. The lowering of the negative conductance for the nonideal profile is immediately apparent. The magnitude of the calculated device Q at 225 GHz is 2.47 for profile 1 and 2.72 for profile 2. The widening of the active region causes a slight downward shift in the frequency where the negative conductance peaks. In general, straggling induced profile grading at the p-n junction will cause some performance degradation which will become more severe at higher frequencies.

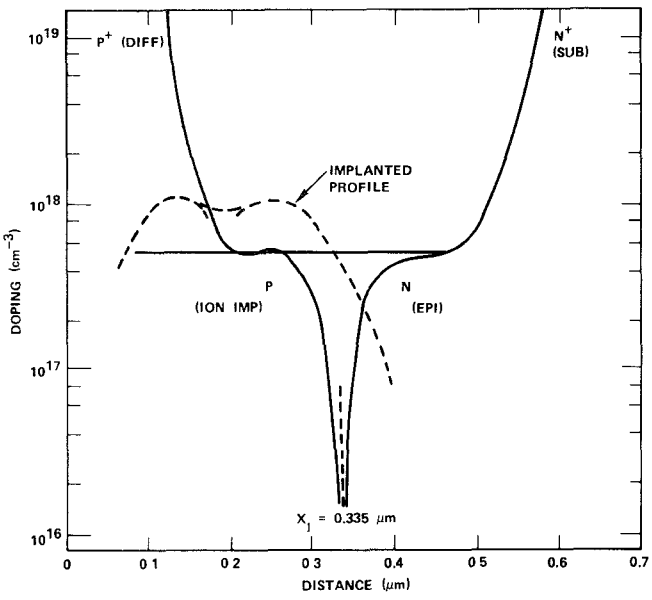


Fig. 6. Ion implantation design for a 225-GHz double-drift IMPATT diode.

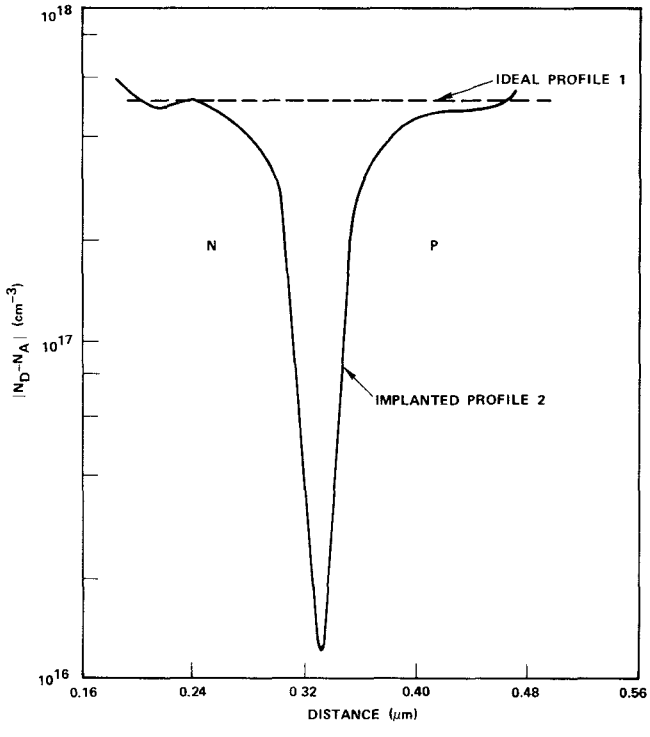


Fig. 7. Idealized and realistic ion implantation profiles.

B. Device Fabrication

The reduction of all sources of positive series resistance is of prime importance in fabricating millimeter-wave IMPATT devices. Two major sources of series parasitic resistance are associated with the substrate and back contact. These are: 1) contact resistance at the substrate–contact metal interface, and 2) series resistance of the substrate modified by skin effects. Contact resistance is

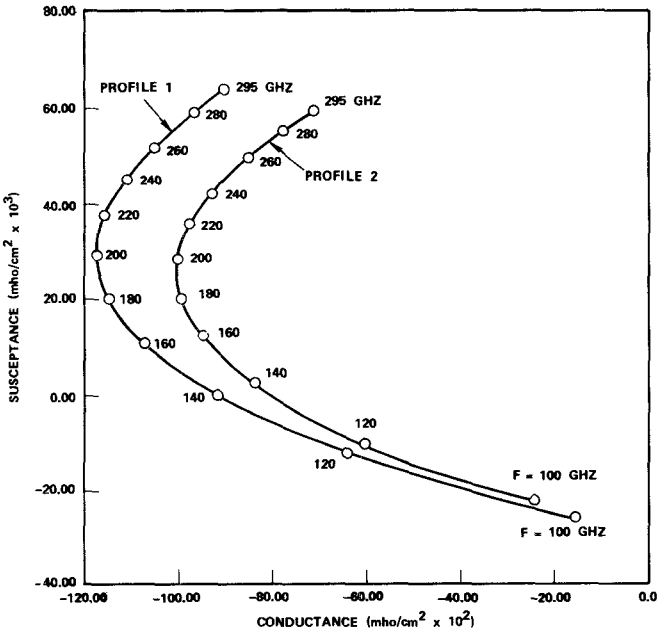
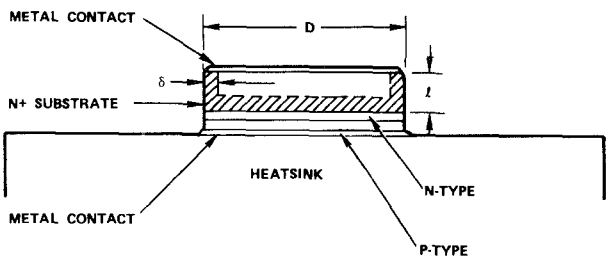


Fig. 8. Calculated diode susceptance and conductance for the profiles of Fig. 7.



FREQUENCY GHz	DIAMETER D (MICRONS)	SKIN DEPTH δ (MICRONS)	RESISTANCE OF CYLINDRICAL SHELL (OHMS)
40	90	7.9	0.049
100	35	5.0	0.21
250	15	3.2	0.85
l = 10 MICRONS SUBSTRATE RESISTIVITY = 0.001 OHM-CM			

Fig. 9. Model for substrate series resistance modified by skin effects.

reduced by maximizing the effective doping level in the substrate at the contact surface either by maintaining a high level of substrate doping ($\sim 10^{20}$ cm^{-3}) or by contact alloying. Minimizing substrate resistivity also reduces the skin effect contribution to series resistance. Fig. 9 illustrates, following De Loach [13], the calculated skin-effect contributions to diode series resistance for several frequencies. To minimize series resistance, the diode substrate must be thinned. Typically, 40-GHz diodes have substrate thickness of 20–30 μm while devices above 200 GHz are thinned to 5–10 μm. Several substrate thinning techniques are commonly employed; bubble etching [14] is particularly convenient. As silicon becomes transparent in the visible region at thicknesses below about 30 μm,

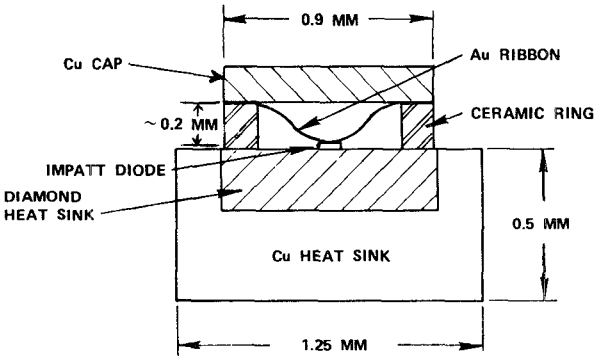


Fig. 10. Sealed ceramic ring—diamond heat-sink diode package.

light transmission is used for final thickness measurement.

Probably the most important area of IMPATT diode fabrication technology relating to device reliability is the contact metallization. All devices described in this work employ a three-component nonalloyed contact metallurgy consisting of 600 Å of chromium, a platinum barrier layer typically 2000 Å in thickness, and an evaporated 3000-Å layer of gold followed by 1–3 μm of plated gold to facilitate thermocompression bonding. Extensive life testing and failure analysis of devices over several years has verified the reliability of this metallurgy.

C. Device Packaging

In general, the package associated with a millimeter-wave IMPATT diode is critical in determining the overall device performance. As the frequency of operation increases, the role of the device package or, more generally, the immediate RF environment of the semiconductor chip becomes more crucial. An improperly designed package can degrade the performance of a device by 1) introducing high RF loss from the packaging material, and 2) having high parasitic capacitances and inductances that force the diode to operate at lower than the optimum design frequency and degrade the diode Q. The features that are necessary for a good CW millimeter-wave IMPATT diode package include:

1) low thermal resistance between the diode chip and the remainder of the circuit;
2) low RF loss from the packaging material;
3) minimal electrical parasitics.

In addition, other desirable physical features are that the package should be:

1) mechanically rugged;
2) hermetically sealable;
3) reproducible.

At higher millimeter frequencies, compromises are necessary among the above package characteristics in order to optimize overall device performance.

As in the other areas of the device technology, there currently exists a demarcation in the approach to millimeter-wave IMPATT packaging at or slightly above 100 GHz. Below this frequency, diodes are packaged in conventional closed, hermetically sealed, and rugged config-

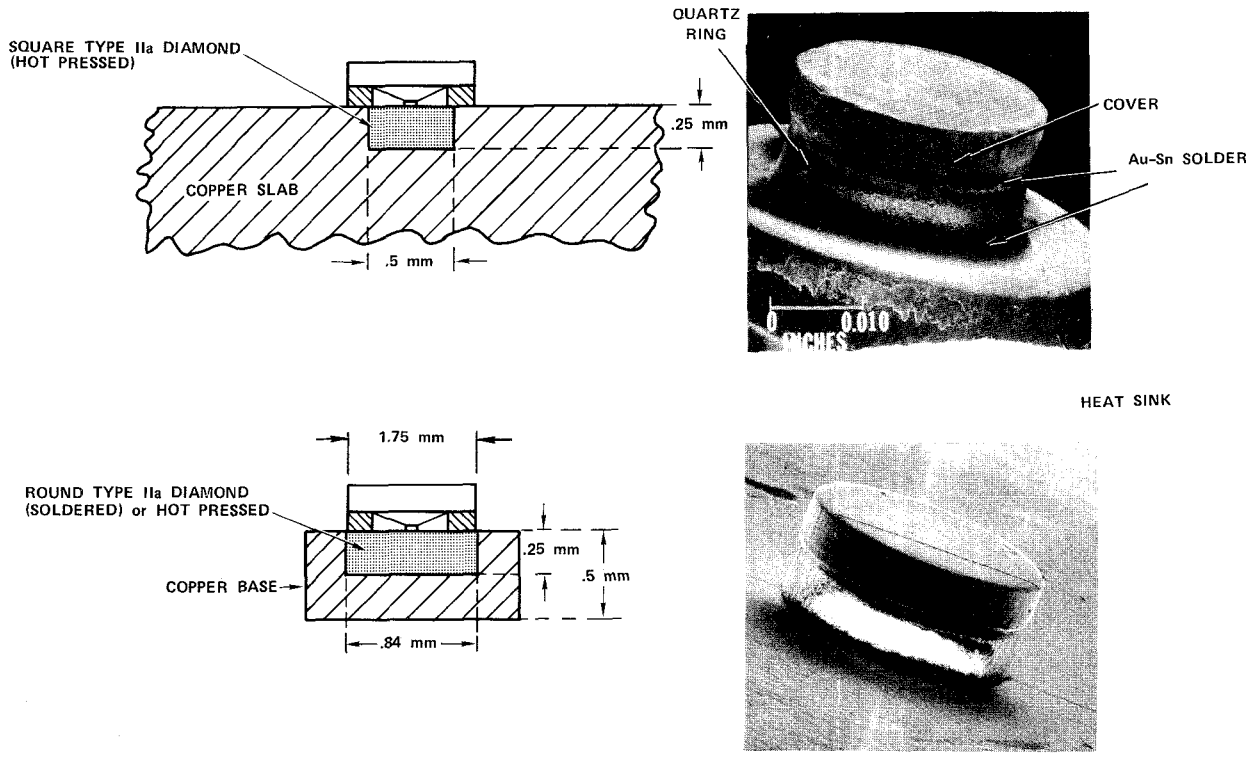


Fig. 11. Sealed quartz ring—diamond heat-sink IMPATT diode packages: (a) pill type; (b) slab type.

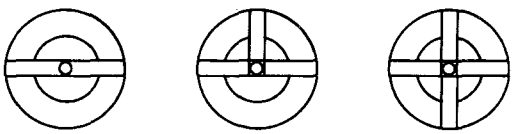


Fig. 12. Ribbon configurations used with quartz ring package: (a) full ribbon; (b) 1 1/2 ribbon; (c) cross ribbon.

urations similar to lower frequency microwave diode packages except for size and choice of materials. At frequencies above 100 GHz, device packages are mostly of the open "quartz standoff" or "wafer" configuration which are not hermetically sealable, are fragile, and are highly labor intensive to assemble. For both types of packages, diamond heat sinking is used to achieve maximum CW device performance. Diamond heat-sinking technology has recently been extended to IMPATT diodes operating at frequencies over 200 GHz. Figs. 10–13 illustrate several examples of CW millimeter-wave IMPATT diode package configurations. Fig. 10 shows a ceramic ring package used for 40-GHz devices. This package incorporates a small round diamond which is soldered or hot pressed into a larger copper cylinder prior to package assembly. Fig. 11 shows a smaller, but similarly configured quartz ring package used for diodes between 50 and 100 GHz. This package is used in a "pill" version (Fig. 11(a)), or may be incorporated into a larger copper slab heat sink which becomes one wall of a waveguide cavity (Fig. 11(b)). The packages shown in Figs. 10 and 11 may have several ribbon configurations, three examples of which are shown in Fig. 12. This allows the package inductance to be varied in order to optimize for particular frequencies or circuit configurations. Open packages which are used with devices above 100 GHz are shown in Fig. 13 which illustrates the single and double standoff diode packages. Also shown are SEM microphotographs of two versions of this package used for devices near or above 200 GHz. The multiple ribbon double standoff shown in Fig. 13(b) has shown very good performance near 220 GHz. Finally, in order to achieve minimal parasitics, a directly contacted diode configuration may be used. This is usually accomplished using a wafer package as shown in Fig. 14.

IV. Oscillator Circuits

A flexible oscillator circuit widely used with IMPATT diodes at millimeter-wave frequencies is the reduced height waveguide cavity shown schematically in Fig. 15. The diode is mounted on the bottom broad wall of the waveguide and is contacted from above by a bias pin. A

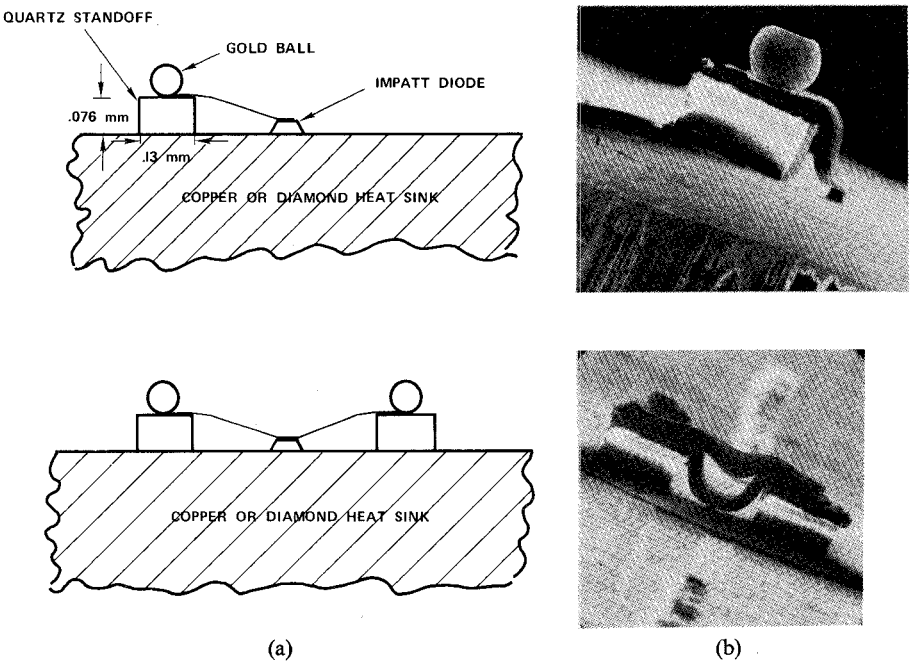


Fig. 13. Quartz standoff package configurations: (a) single standoff; (b) double standoff.

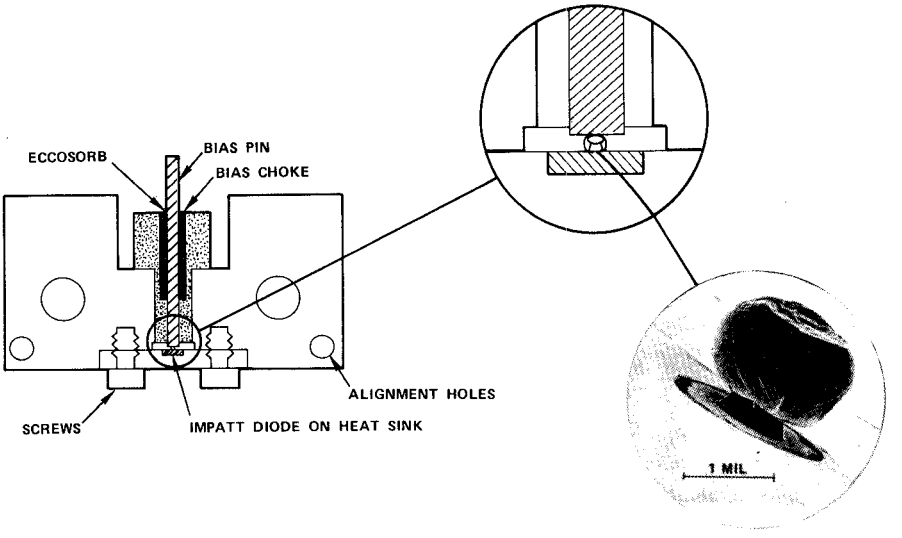


Fig. 14. Wafer-mounted directly contacted diode.

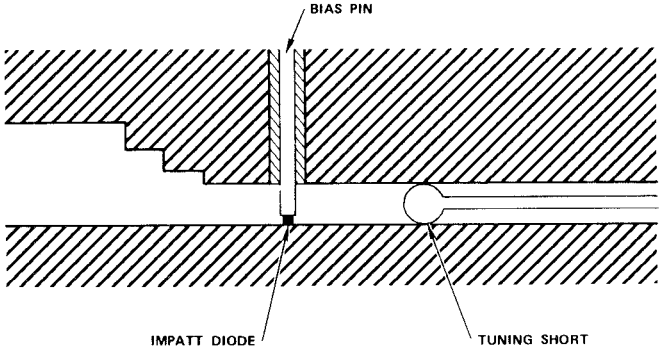


Fig. 15. Reduced height waveguide cavity.

tuning short is located in the waveguide on one side of the IMPATT. On the other side a multistep transformer (or a taper) provides a transformation to the full height waveguide output. Variations of this circuit have a coaxial section with the bias pin as center conductor located in either the top or bottom broad wall and cross-coupled to the waveguide. Cavities of this type have been modeled by Fong *et al.* [15]. Fig. 16 shows a cavity which has been used at Q band (33–50 GHz). Here the diode is recessed into a two-step coaxial section in the bottom waveguide wall. At higher millimeter-wave frequencies, the approach is modified by forming the cavity in several sections. One such Y-band (170–260 GHz) cavity is shown in Fig. 17

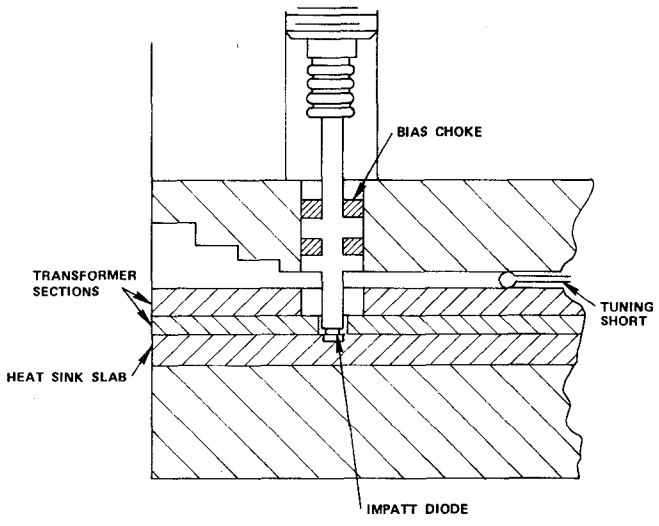


Fig. 16. Cross section of a Q-band (33–50-GHz) IMPATT oscillator circuit.

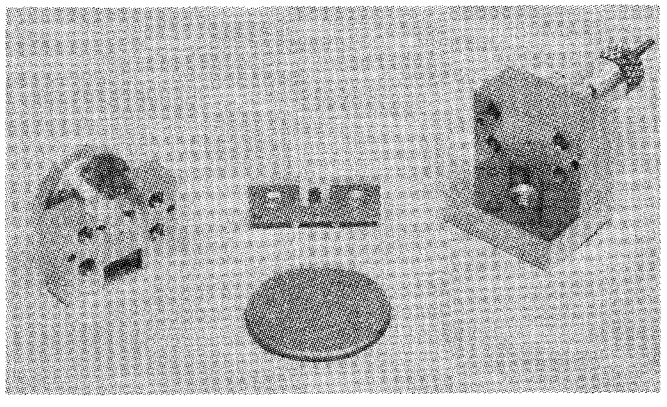


Fig. 17. Waveguide IMPATT cavity for use at Y band (170–260 GHz) which employs a wafer mounted diode.

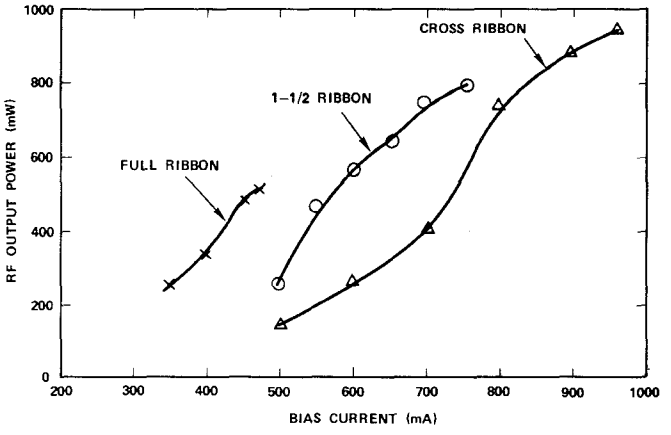


Fig. 18. Output power as a function of bias current for diodes with three different package ribbons variations.

TABLE IV
RF PERFORMANCE OF SILICON DDR IMPATT's/CW OSCILLATORS

Frequency (GHz)	Package Type	Output Power (W)	Efficiency (%)	Estimated Junction Temperature (°C)
40.1	Ceramic Ring. Full Ribbon	1.52	12.9	250
40.1	Ceramic Ring. Full Ribbon	2.26	10.6	440 (Near Burnout)
60.5	Quartz Ring Half Ribbon	1.2	6.0	250
93.6	Quartz Ring Full Ribbon	0.58	5.8	275
91.9	Quartz Ring Cross Ribbon	0.98	3.6	475 (Near Burnout)
220.5	Two Quartz Standoff	0.050	1.0	360
228.0	Two Quartz Standoff	0.033	0.8	340

TABLE V
EFFECT OF RIBBON CONFIGURATION

Ribbon Configuration	Zero-Bias Capacitance (pF)	Bias Current (mA)	Frequency (GHz)	Output Power (Watt)	Efficiency (%)	Estimated ΔT_j (°C)
Full	1.24	471	94.4	0.52	5.1	263
1-1/2	1.78	756	95.0	0.79	4.6	337
Cross	1.95	963	94.7	0.94	4.1	394

[16]. It consists of three major sections: a tapered transformer, a reduced height waveguide wafer section into which the IMPATT is mounted, and a section containing a tuning short. The use of the wafer module facilitates the contacting of the packaged or unpackaged IMPATT with the bias pin at those frequencies where the diode and circuit geometries are extremely small.

V. RF RESULTS

We have operated CW IMPATT's in oscillator circuits at frequencies as high as 250 GHz. Testing was generally carried out in reduced height waveguide cavities of the types described earlier. Test data for millimeter-wave DDR diodes mounted on diamond heat sinks are given in Table IV. Power measurements were relatively straightforward at frequencies below 100 GHz where calibrated thermistor mounts were used. Power measurements above 200 GHz were carried out using an E-band (WR-12) dry calorimeter with appropriate waveguide transitions.

Devices operated below 100 GHz were generally assembled in sealed disk-type packages. It was found empirically that details of the package geometry can have a large influence on performance. For instance, near 94 GHz, the full, 1 1/2, and cross ribbon configurations for the quartz ring package described in Section III-C were all investigated. The general trend was to larger area diodes and greater saturated output power as the total ribbon inductance decreased. However, the higher power was accompanied by increased junction temperature and decreased efficiency. This result is indicated in Fig. 18 in which are plotted output power versus bias current for three diodes from the same lot, each one with a different ribbon configuration. Each diode was tested in a 0.38-mm reduced height cavity. Further data on the same diodes are given in Table V.

At frequencies exceeding 200 GHz, the packaging parameters become extremely critical with respect to their

effect on RF performance. Most devices at these frequencies were assembled in open quartz standoff packages. Best results in terms of output power were achieved with the two standoff package shown in Fig. 13(b).

VI. Reliability

Reliability testing has been an important adjunct to the process development of millimeter-wave silicon IMPATT's. Step-stress reliability life tests have been periodically carried out on groups of DDR IMPATT's. In a step-stress test, devices are operated for a fixed period of time at each of a series of increasing junction temperature levels until all fail. For the IMPATT's the appropriate temperatures were achieved by internal power dissipation. Tests of this type are very useful for obtaining a rapid assessment of the diode lot quality.

Recent step-stress tests carried out on DDR IMPATT's on type-IIA diamond heat sinks have revealed that the predominant failure mechanism was similar to the "internal channel" described by Sellberg *et al.* [17]. The failures occurred when the formation of a gold–silicon alloy spike in the bulk of the device resulted in a junction short. Further accelerated testing is needed in order to obtain reasonable quantitative estimates of diode life expectancy for recent DDR diodes under normal operating conditions. However, accelerated life tests previously carried out on SDR devices indicated a similar failure mechanism and led to a predicted median-time-to-failure of approximately 2×10^6 h at 200°C [18].

VII. Summary and Prognosis

Currently, flat profile double-drift silicon IMPATT diodes provide an effective means for the solid-state generation of millimeter-wave power from 30 to over 250 GHz. These diodes, incorporating diamond heat-sinking technology, provide single device CW power levels on the order of 1–2 W at 35 and 60 GHz, nearly 1 W at 94 GHz, and 50 mW near 220 GHz. These performance figures are a result of careful attention to a number of critical areas of device processing including junction formation, substrate thinning, and the reduction of parasitic contact resistance. In addition, several aspects of device packaging, for example, the control of parasitic reactances and the minimization of thermal resistance, also play a very important role in device performance, particularly at higher frequencies (> 100 GHz). In the latter area, special low parasitic packaging configurations have been developed.

Below about 100 GHz, silicon IMPATT diode technology is maturing. All devices in this frequency range are fabricated and packaged with a common technology which is similar in many respects to that of lower frequency (microwave) devices. Above 100 GHz, diodes are more difficult to fabricate and package and at present fall into the category of laboratory devices. While limited reliability data are available from accelerated testing of diodes designed to operate below 100 GHz, no such work has yet been done with higher frequency devices.

In the future, further optimization of device profiles above 100 GHz is required. Hyperthin device fabrication technology based on preferential etching techniques should result in moderate performance improvements. Further work on low and controlled parasitic package configurations will result in improved device performance throughout the millimeter spectrum, but particularly above 100 GHz. Continued effort on circuit design is required in order to suppress the variety of instabilities [19] associated with large-signal IMPATT diode operation. As the device technology matures, increased attention is being given to millimeter-wave power combining. At lower frequencies, both chip [20] and circuit [21] level approaches are being pursued. Although there is evidence to suggest that resonant cavity circuit techniques [21] are usable to at least 100 GHz, the entire area of power combining at higher frequencies is presently open and probably awaits the development of new technology such as quasioptical techniques. In the near term (1–3 years), a significant amount of new reliability data for CW double-drift devices on diamond heat sinks will be generated at 40, 60, and 94 GHz. Definative reliability data at higher frequencies will be slower in coming and to some degree will await further maturing of the device technology.

Acknowledgment

The authors acknowledge the contributions of E. Nakaji, R. Ying, F. Fischer, M. Padilla, A. Martin, F. Thrower, D. Lee, H. Lucky, and N. Conners in processing and packaging IMPATT diodes, and the assistance of C. Chao, K. Weller, G. Oransky, G. Watanabe, M. Morishita, Y. Ma, D. English, T. Fong, C. Ito, and E. Athey in diode and oscillator characterization and evaluation.

References

[1] T. T. Fong and H. J. Kuno, "Millimeter-wave pulsed IMPATT sources," this issue, pp. 492–499.

[2] D. L. Scharfetter, W. J. Evans, and R. L. Johnston, "Double-drift-region (p^+pnn^+) avalanche diode oscillators," *Proc. IEEE* (Lett.), vol. 58, pp. 1131–1133, July 1970.

[3] T. E. Seidel, R. E. Davis, and D. E. Iglesias, "Double-drift-region ion-implanted millimeter-wave IMPATT diodes," *Proc. IEEE*, vol. 59, pp. 1222–1228, Aug. 1971.

[4] D. L. Scharfetter and H. K. Gummel, "Large-signal analysis of a silicon Read diode oscillator," *IEEE Trans. Electron Devices*, vol. ED-16, pp. 64–77, Jan. 1969.

[5] F. A. Blum and N. B. Kramer, "Frequency scaling of IMPATT diodes," *IEEE Trans. Electron Devices*, vol. ED-17, pp. 983–986, Nov. 1970.

[6] T. Misawa, "Negative resistance in p-n junctions under avalanche breakdown conditions, Parts I and II," *IEEE Trans. Electron Devices*, vol. ED-13, pp. 137–151, Jan. 1966.

[7] ——, "Multiple uniform layer approximation in analysis of negative resistance in p-n junction in breakdown," *IEEE Trans. Electron Devices*, vol. ED-14, pp. 795–808, Dec. 1967.

[8] C. Canali *et al.*, "Electron and hole drift velocity measurements in silicon and their empirical relation to electric field and temperature," *IEEE Trans. Electron Devices*, vol. ED-22, pp. 1045–1047, Nov. 1975.

[9] G. Ottaviani, "Correction to 'Electron and hole drift velocity

measurements in silicon and their empirical relation to electric field and temperature,'" *IEEE Trans. Electron Devices*, vol. ED-23, p. 1113, Sep. 1976.
[10] W. N. Grant, "Electron and hole ionization rates in epitaxial silicon at high electric fields," *Solid-State Electron.*, vol. 16, pp. 1189–1203, 1973.
[11] K. Board, "Thermal properties of annular and array geometry semiconductor devices on composite heat sinks," *Solid-State Electron.*, vol. 16, pp. 1315–1320, 1973.
[12] D. L. English, E. M. Nakaji, and R. S. Ying, "Improved performance of millimetre-wave IMPATT diodes on type-IIa diamond heat sinks," *Electron. Lett.*, vol. 12, pp. 675–676, Dec. 9, 1976.
[13] B. C. DeLoach, Jr., "Thin Skin IMPATT's," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-18, pp. 72–74, Jan. 1970.
[14] A. I. Stoller, R. F. Speers, and S. Opresko, "A new technique for etch thinning silicon wafers," *RCA Rev.*, vol. 31, pp 265–271, June 1970.
[15] T. T. Fong, K. P. Weller, and D. L. English, "Circuit characterization of *V*-band IMPATT oscillators and amplifiers," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-24, pp. 752–758, Nov. 1976.
[16] C. Chao, R. L. Bernick, E. M. Nakaji, R. S. Ying, K. P. Weller, and D. H. Lee, "*Y*-band (170–260 GHz) tunable CW IMPATT diode oscillators," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-25, pp. 985–991, Dec. 1977.
[17] F. Sellberg, P. Weissglas, and G. Andersson, "A study of failure mechanisms in silicon IMPATT diodes," *IEEE Trans. Electron Devices*, vol. ED-25, pp. 742–746, June 1978.
[18] N. B. Kramer, "Millimeter wave semiconductor devices," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-24, pp. 685–693, Nov. 1976.
[19] Y. Hirachi, T. Nakagami, Y. Toyama, and Y. Fukukawa, "High-power 50-GHz double-drift-region IMPATT oscillators with improved bias circuits for eliminating low frequency instabilities," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-24, pp. 731–737, Nov. 1976.
[20] N. W. Cox, G. N. Hill, J. W. Amos, and C. T. Rucker, "Series interconnection of six TRAPATT devices on a diamond substrate," in *1976 IEEE Int. Microwave Symp. Dig.*, pp. 45–47.
[21] F. J. Bayuk and J. E. Raue, "*Ka*-band solid state power amplifier," in *1977 IEEE Int. Microwave Symp. Dig.*, pp. 29–31.

Millimeter-Wave Pulsed IMPATT Sources

T. T. FONG, MEMBER, IEEE, AND H. J. KUNO, FELLOW, IEEE

Invited Paper

***Abstract*—High-power millimeter-wave pulsed IMPATT sources have found a variety of applications as solid-state transmitters in radar applications. These applications have been greatly enhanced by the rapidly advancing millimeter-wave technology of which the high-power pulsed IMPATT source is a key element. In this paper the unique IMPATT properties which affect the oscillator spectral purity and coherency are reviewed. Some key considerations for the device design and system applications of the pulsed oscillators are discussed along with the state of the art, recent progress, and future trend.**

I. Introduction

AFTER A LONG, slow start, millimeter-wave systems development has been recently increasing at a rapid rate. A wide range of systems are now under development. Examples are tracking radar, missile seekers, radiometers, and short range communications. Millimeter-wave systems offer many advantages over both microwave systems and electrooptical systems. In comparison with microwave systems, millimeter-wave systems offer smaller size, lighter weight, improved accuracy, greater resolution, and smaller antenna size. Furthermore, in comparison with electrooptical or infrared systems, millimeter-wave systems provide greatly improved penetration through cloud, smoke, and dust. Most of the current activities for millimeter-wave systems are centered around 35 and 94 GHz, where atmospheric attenuation is relatively low. Development activities in the 140-GHz range, which is the next low atmospheric attenuation window, is now underway. The exploratory work now extends to a frequency as high as 240 GHz.

A key element in many millimeter-wave systems is the solid-state pulsed sources. These sources, because of their small size, light weight, and low voltage power supply requirements, are now finding applications as transmitters in many radar systems. In this paper, the state-of-the-art performance of millimeter-wave pulsed IMPATT oscillators is reviewed with in-depth discussion of the recent development and trend. Design and system application considerations that are unique to pulsed IMPATT oscillators are discussed. Design considerations for both diode and circuit, such as the strong temperature dependence of the diode impedance which results in frequency chirp during pulse, are covered. Methods for controlling the frequency chirp characteristics, phase and injection locking characteristics, and noise performance of transmitters

Manuscript received June 16, 1978; revised November 29, 1978.

T. T. Fong is with the Hughes Aircraft Company, Electron Dynamics Division, Torrance, CA 90509.

H. J. Kuno is with the Hughes Aircraft Company, Solid-State Subsystems Department, Torrance, CA 90509.

0018-9480/79/0500-0492$00.75 ©1979 IEEE